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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/878,554	CHEN ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☒ Claim(s) *1-7 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

1. The abstract of the disclosure is objected to because the abstract exceeds 150 words in length. Correction is required. See MPEP § 608.01(b).

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: '911' and '931' in Figure 9; '1320', '1321', '1322', '1330', '1331', '1332', '1341', '1342', '1350', '1351' and '1352' in Figure 13; and '1431', '1432', '1433', '1434' and '1435' in Figure 14. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the

Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 1-7 and 9 are objected to because of the following informalities: claims 1 and 9 do not end with a period.

Claims 2-7 depend from claim 1; hence inherit the deficiencies of claim 1.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Maruyama, Daisuke (US 6205567 B1).

35 U.S.C. 102(e) rejection of claim 1.

Maruyama teaches that in an integrated circuit (IC) having at least one fault to be tested by fault simulation using at least one test (the IC of Figure 8 in Maruyama is an IC

having at least one fault to be tested by fault simulation using at least one test; see Abstract in Maruyama; Note: col.1, lines 40-45 in Maruyama teach fault simulation is performed on the basis of the assumption that there will be one fault), each of said tests including at least one input test vector (see Step S2 in Figure 2 of Maruyama), a method for improving the efficiency of the fault simulation (see Abstract in Maruyama) comprising the steps of: a) performing a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC (col. 14, lines 29-34 in Maruyama teach that a true-value simulation is performed for the i^{th} test; col. 3, lines 42-45 in Maruyama teach that a true-value simulator performs true-value simulation in a true state-where there is not any fault, i.e. a true value simulation is a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC; col. 14, lines 29-34 in Maruyama teach that the address and true-value for each node are stored in a table in memory; Figure 4 in Maruyama teaches that simulation is performed for each storage element to which a fault event is propagated, i.e., the storage elements are internal nodes of the IC at which faults are detected by comparing the results of the true value simulation with results from the fault simulation; hence Maruyama teaches performing a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC); b) based on said good machine simulation, identifying faults in said IC that are potentially tested by said at least one test (col. 1, lines 45-48 in Maruyama teach that a list of faults is provided; col. 19, lines 23-25 in Maruyama teach that faults are then injected into the IC during fault simulation; col. 3, lines 45-50 in Maruyama teach that a fault is detected on the basis of

a difference between a result of the real-value simulation and a result of the fault simulation; col. 5, lines 63-65 in Maruyama teach that undetectable faults are present in the list of faults; hence the list of faults identify faults that are potentially tested by said at least one test); c) with said at least one test, performing a fault simulation on said faults that were identified as potentially tested (col. 3, lines 45-50 in Maruyama teach that a fault is detected on the basis of a difference between a result of the real-value simulation and a result of the fault simulation); and d) repeating steps a) through c) for each of said at least one test (Figure 2 teaches n tests for repeating steps a to c).

35 U.S.C. 102(e) rejection of claim 2.

Maruyama teaches backtracing from each observable node, said backtrace through each of said internal nodes being based on said fault-free circuit simulation (col. 9, lines 37-45 in Maruyama teach backtracing from each observable node, said backtrace through each of said internal nodes being based on said fault-free circuit simulation) and being limited to paths along which a faulty value has a possibility of propagating to said observable node (col. 5, lines 5-14 in Maruyama teach only paths capable of propagating a faulty value to said observable node are activated).

35 U.S.C. 102(e) rejection of claim 3.

Figure 1 of Maruyama is a test generator for generating tests in the Maruyama patent using a true-value simulator and a fault simulator.

35 U.S.C. 102(e) rejection of claim 4.

The Abstract of Maruyama teaches that the test in the Maruyama patent is for combinational circuits, i.e., circuits using only logical elements; hence the true-value simulator is a logic simulator.

35 U.S.C. 102(e) rejection of claim 6.

Col. 5, lines 59-65 in Maruyama teaches that an activation path is activated and becomes able to detect a fault at the time of detection of the fault.

35 U.S.C. 102(e) rejection of claim 7.

Observable nodes are sequential circuits such as flip-flops (Note: flip-flops inherently are latches; col. 2, lines 26-38 of Maruyama). Col. 10, lines 50-65 teach the use of ROM and RAM.

35 U.S.C. 102(e) rejection of claim 8.

Maruyama teaches that in an integrated circuit (IC) having at least one fault to be tested by fault simulation using at least one test (the IC of Figure 8 in Maruyama is an IC having at least one fault to be tested by fault simulation using at least one test; see Abstract in Maruyama; Note: col.1, lines 40-45 in Maruyama teach fault simulation is performed on the basis of the assumption that there will be one fault), each of said tests including at least one input test vector (see Step S2 in Figure 2 of Maruyama), a method for improving the efficiency of the fault simulation (see Abstract in Maruyama)

comprising the steps of: a) performing a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC (col. 14, lines 29-34 in Maruyama teach that a true-value simulation is performed for the i^{th} test; col. 3, lines 42-45 in Maruyama teach that a true-value simulator performs true-value simulation in a true state-where there is not any fault, i.e. a true value simulation is a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC; col. 14, lines 29-34 in Maruyama teach that the address and true-value for each node are stored in a table in memory; Figure 4 in Maruyama teaches that simulation is performed for each storage element to which a fault event is propagated, i.e., the storage elements are internal nodes of the IC at which faults are detected by comparing the results of the true value simulation with results from the fault simulation; hence Maruyama teaches performing a good machine simulation on said IC with said at least one test to obtain values of each internal node of said IC); b) based on said good machine simulation, identifying faults in said IC that are blocked by said at least one test from being observed at an observable point of said IC (col. 11, lines 19-25 of Maruyama teach a flag for indicating undetected faults; Note: undetected faults are blocked faults); c) with said at least one test, performing a fault simulation on said faults that were identified as not being blocked (col. 3, lines 45-50 in Maruyama teach that a fault is detected on the basis of a difference between a result of the real-value simulation and a result of the fault simulation; Note: only a detectable or non-blocked fault can propagate a result of the fault simulation that would make the fault detectable); and d) repeating

steps a) through c) for each of said at least one test (Figure 2 teaches n tests for repeating steps a to c).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 5, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maruyama, Daisuke (US 6205567 B1).

35 U.S.C. 103(a) rejection of claim 5.

Maruyama, substantially teaches the claimed invention described in claims 1-4 (as rejected above).

However Maruyama, does not explicitly teach the specific use of a hardware fault simulator.

The Examiner asserts that use of a hardware fault simulator versus a software implemented fault simulator or any combination thereof would have been based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Maruyama by including use of a hardware fault simulator. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that a hardware fault simulator would have provided the opportunity to implement the test device in the Maruyama patent based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

35 U.S.C. 103(a) rejection of claim 9.

Claim 9 is a software implementation of the limitations in claim 8 containing all of the limitations of claim 8 except for the software implementation of those limitations.

Maruyama, substantially teaches the claimed invention described in claim 8 (as rejected above).

However Maruyama, does not explicitly teach the specific use of a software implementation for the limitations in claim 8.

The Examiner asserts that use of a software implementation for the limitations in claim 8 versus a hardware implementation for the limitations in claim 8 or any combination thereof would have been based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Maruyama by including use of a software implementation for the limitations in claim 8. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a software implementation for the limitations in claim 8 would have provided the opportunity to implement the test device in the Maruyama patent based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

35 U.S.C. 103(a) rejection of claim 10.

Claim 10 is a software implementation of the limitations in claim 1 containing all of the limitations of claim 1 except for the software implementation of those limitations. Maruyama, substantially teaches the claimed invention described in claim 1 (as rejected above).

However Maruyama, does not explicitly teach the specific use of a software implementation for the limitations in claim 1.

The Examiner asserts that use of a software implementation for the limitations in claim 1 versus a hardware implementation for the limitations in claim 1 or any combination thereof would have been based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Maruyama by including use of a software implementation for the limitations in claim 1. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a software implementation for the limitations in claim 1 would have provided the opportunity to implement the test device in the Maruyama patent based on basic engineering design choice taking into consideration available space for circuitry, speed requirements (Note: hardware is generally faster than software) and flexibility (Note: software is more flexible than hardware).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Shigeta, Kazuki (US 6301685 B1) teaches an error propagation

path extraction system for quickly obtaining a signal line in which a fault may propagate in a combinational logic circuit. Snethen, Thomas J. (US 3961250 A) teaches a simulator oriented fault test generator for testing complex integrated circuits.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.

Joseph D. Torres, PhD
Art Unit 2133